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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,737	ZHAO ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,11 and 15* is/are rejected.

7)☒ Claim(s) *3-5, 7-9,12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' election of group I filed on 10/29/04 without traverse is acknowledged. Claim 1 is generic to species I and II, therefore, if claim 1 is found allowable, claim 10 could be rejoined. The applicant explicitly admits that species III is not patentably distinct from species I (response on 10/29/04, page 4), therefore, the restriction requirement to species III is withdrawn. The following is a detailed Office action of claims 1-9 and 11-15.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves

modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

The disclosure is objected to because of the following informalities: (i) it compares the invention with the prior art, (ii) it uses words which can be implied, i.e., "is disclosed".

Appropriate correction is required.

Claim Objections

3. Claims 2, 4, 7-9, 13 and 15 are objected to because of the following informalities:

In claim 2, line 4, "source node" should be changed to -- common source node -- to avoid potential antecedent basis problem because there are source node of first branch, source node of second brand, common source node,

line 8, the same problem exists regarding the term "source node",

lines 8-9, "a high potential" should be changed to -- said high potential --, see lines 4-5.

In claim 4, line 2, "said latch" should be changed to -- said latches --, see line 1.

In claim 7, line 3, "received" should be changed to -- receiving --,

line 6, "one said NAND input" should be changed to -- the other one of said NAND input --.

In claims 8-9, lines 4, the terms "data signal inverter input" should be changed to -- data inverter input --.

In claim 13, line 2, "said latch" should be changed to -- said latches --, see line 1.

In claim 15, line 3, "transistors", first occurrence, should be changed to -- transistor --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,036,217, issued to Rollins et al.

As per claim 1, Rollins discloses a flip-flop circuit (Fig. 1B) comprising:

(a) a first branch having two transistors in series (transistors 202 and 206) and a source node (226);

(b) a second branch having two transistors in series (transistors 204 and 208) and a source node (226), said source node being common with said source node of said first branch (node 226);

(c) a shared transistor (transistor 210) having its source connected to said source nodes of said first and second branches (the common source node 226); and

(d) a pulse generator (not shown, the circuit which generates the clock signal CLOCK. Note that the clock signal CLOCK is seen as a pulse signal because for each period of the cycle, there is a pulse. The pulse width of the pulse can be smaller than 50 percent, 50 percent or larger than 50 percent. Cited in the enclosed PTO-892, DiTommaso, US Patent No. 6,271,701 shows in Fig. 2 a clock signal which has pulse width less than 50 percent) connected to the gate of said shared transistor (210).

As per claim 2, Rollins further discloses:

(a) the first branch comprises a P type transistor (202) and an N type transistor (206) connected in series (as shown), the source of said N type transistor (206) being connected to said common source node (226) and the drain of said P type transistor (202) being connected to a high potential (VDD); and

(b) the second branch comprises a P type transistor (204) and an N type transistor (208) connected in series, the source of said N type transistor (208) being connected to said common source node (226) and the drain of said P type transistor (204) being connected to said high potential (VDD).

As per claim 6, as shown, the Rollins shared transistor 210 is an N type transistor.

5. Claims 11 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Rabaey, "Designing Sequential Logic Circuits", Nov. 2000 (cited in IDS).

As per claim 11, Rabaey discloses a static explicit pulsed flip-flop circuit (Fig. 7.35, page 297) comprising:

(a) a first branch having three transistors in series (transistors M1-M3), one of said first branch transistors being a clocked transistor (M2) and the other two transistors (M1 and M3) being non-clocked transistors having their gates connected to a data input (D);

(b) a second branch having three transistors in series (transistors M3-M6), one of said second branch transistors being a clocked transistor (M5) and the other two transistors (M4 and M6) being non-clocked transistors having their gates connected to a node between said first branch non-clocked transistors (as shown); and

(c) a pulse generator (Fig. 7.35b) connected to the gates of said clocked transistors in the first and second branches.

As per claim 15, Rabaey further discloses:

(a) the first branch clocked transistor (M2) and the second branch clocked transistor (M5) are N type transistors (as shown);

(b) one of said non-clocked first branch transistors is a P type transistor (M3), one of said non-clocked first branch transistors is an N type transistor (M1), and said first branch N-type transistor is connected to said first branch clocked transistor (M1 and M2 are connected); and

(c) one of said non-clocked second branch transistors is a P type transistor (M6), one of said non-clocked second branch transistors is an N type transistor (M4), and said second branch N-type transistor is connected to said second branch clocked transistor (M4 and M5 are connected).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rabaey, "Designing Sequential Logic Circuits", Nov. 2000 (cited in IDS).

As per claim 1, Rabaey discloses a flip-flop circuit having a structure discussed in claim 11 herein above. Rabaey does not explicitly disclose the clocked transistor (M2 and M5) being shared by the first and second branches as called for in the claim.

In the response to the election requirement filed on 10/29/04, the applicant explicitly admits that species I and III are not patentably distinct (response on 10/29/04, page 4).

It would have been obvious to one skilled in the art at the time of the invention was made to use a single transistor for receiving the clock signal in the first and second branch as admitted by the applicant that they are not patentably distinct. The motivation would be to reduce the number of transistors in the flip-flop circuit by using a single transistor to receive the clock signal instead of two transistors.

As per claim 2, the modified flip-flop circuit discussed in claim 1 clearly has the structure recited in the claim.

As per claim 6, because M2 and M5 are N type transistors, the shared transistor would be N type transistor.

Allowable Subject Matter

7. Claims 3-5 and 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3-5 and 9 are allowable because the prior art of record fails to disclose or suggest the inclusion of first and second branch latches connected to the sources of the first branch P type transistor and the second branch P type transistor, respectively, as recited in claim 3.

Claim 7 is allowable because the prior art of record fails to disclose or suggest the inclusion of an inverter chain, a NAND and an inverter connected as recited in a pulse generator.

Claim 8 is allowable because the prior art of record fails to disclose or suggest the inclusion of a data signal input connected to the gates of the P and N type transistors in the first branch and a data inverter connected as recited in the claim.

Claims 12-14 are allowable for the reason noted in claim 3.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

12/22/04

Minh Nguyen
Primary Examiner
Art Unit 2816